REMARKS/ARGUMENTS

The Applicant has carefully considered this application in connection with the Examiner's Final Action and respectfully requests reconsideration of this application in view of the foregoing amendments and the following remarks. The Applicant originally submitted Claims 1-20 in the application. Claims 1, 8 and 15 are amended in this response to present the claims in better form for appeal. Accordingly, Claims 1-20 are currently pending in the application.

I. Rejection of Claims 1-20 under 35 U.S.C. § 103(a)

The Examiner rejected Claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,784,603 to Leung, *et al.*, in view of U.S. Patent 4,910,664 to Arizono, *et al.* The Examiner admitted previously that Leung fails to teach the elements of Claims 1, 8 and 15, "a loop recognizer ... that determines whether a loop is present in fetched instructions an reinstates a validity of instructions in said loop and prevents said prefetch circuitry from prefetching instructions outside of said loop until said loop completes execution", but asserted that Arizono cures this deficiency of Leung. The Applicant traversed this rejection in the previous response, and the Examiner has sustained the rejection. For the reasons set forth below, this combination does not teach or suggest each and every element of the presently claimed invention, and is thus not a proper combination.

First addressing the element of preventing prefetch outside of the loop, the Examiner states in § 9 of the Office Action that Arizono, column 3, lines 10-67 and column 5, lines 43-54 teach, "The prefetch counter is reset to the loop-beginning address each time the prefetch counter equals the loop-ending address, thereby preventing said prefetch circuitry from prefetching instructions outside of said loop until said loop completes processing." However, column 5 line 64 through column 6

line 2, and FIGURE 5, state 4, teach that because the instruction bus is 16 bits wide, a byte fetch may result in the fetch of an additional byte past the end of the loop, which is then discarded when the prefetch counter is reset to the beginning of the loop. Thus, Arizono does not prevent the prefetch circuitry from prefetching instructions "outside of said loop until said loop completes execution," and Arizono fails to teach this limitation. Therefore the combination of Leung and Arizono fails to teach each limitation of independent Claims 1, 8 and 15, and these claims are allowable. Additionally, each claim depending from these claims is allowable.

Moreover, Claim 1 also contains the limitation that states, "...a loop recognizer ... that determines whether a loop is present in fetched instructions and reinstates a validity of said fetched instructions in said loop...." In the previous response, the Applicant noted that ¶39 of the Specification states, "the loop recognizer 330 reinstates the validity of the instructions in the loop (via the cache line valid bit...)." Continuing, the Applicant argued,

> When executing such a loop, a processor constructed according to the teachings of the present invention will not only confine any prefetch to instructions in the loop, but will advantageously disable a prefetch when the required instructions are resident in the instruction cache memory. This provides the advantage that prefetching of instructions is reduced during loop execution, reducing the consumption of power associated with the prefetch. In the extreme, when the loop is small enough to entirely fit within the instruction cache memory, no instruction prefetch at all is necessary after the first prefetch.

In response, the Examiner argues in § 10 of the Office Action that Arizono teaches reinstating the validity of prefetched instructions, stating,

> ...Arizono has in fact taught that the validity of prefetched instructions are [sic] reinstated. In Arizono, resetting the prefetch counter to the loop-beginning address reinstates the validity of the prior instructions in the loop that are stored in the *loop buffer* (Column 3, Lines 10-67, column 5, lines 43-54) (emphasis added).

However, Arizono does not teach a "loop buffer." Arizono improves the performance of execution of a while loop by resetting the prefetch counter to a stored loop-beginning address to avoid the expense of repeated calculation of the loop-beginning address at the end of each loop (Column 3, lines 10-15, Column 5, lines 54-63), but there is no teaching of storage of instructions in a loop buffer. FIGURE 2 shows a register block 5, but its disclosed function is limited to storage of the program counter, loop-begin address and loop-end address. Because Arizono provides no loop buffer to store the instructions, the Examiner's argument is erroneous.

If the Examiner intended to refer to instructions stored in an instruction cache memory (not specifically taught, but inherent by virtue of instruction prefetch), then the Examiner is still not correct. In reinstating a validity of instructions, at best Arizono teaches the reinstatement of the validity of instructions in the abstract sense, *i.e.*, returning to the top of the loop in the computational algorithm. Such a teaching is trivial and well known to those skilled in the art. An element of Claims 1, 8 and 15 is the *specific* reinstatement of the validity of instructions residing in the instruction cache to obviate the need to fetch these instructions again ("...reinstates a validity of said fetched instructions..."). Nowhere is this limitation taught or suggested by Arizono.

For these reasons, Arizono fails to cure the deficiency of Leung, and the combination cited by the Examiner is improper. Thus, independent Claims 1, 8 and 15, and those depending from them, are allowable.

III. Conclusion

In view of the foregoing amendments and remarks, the Applicant now sees all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-20.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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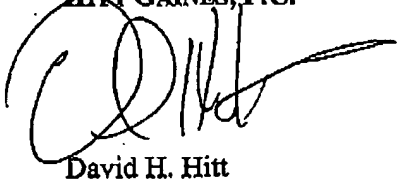

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